REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-78 are in the application. Claims 1-38 are subject to examination and claims 39-76 have been withdrawn from examination. Claims 1, 6, 20, and 25 have been amended. New dependent claims 77 and 78 have been added.

The features added to new claims 77 and 78 relate to the structural hardware unit being configured for access to the memory device independently of the intelligent core as described on page 11, line 23 to page 12, line 4 and page 12, lines 6-14 of the instant specification.

In item 3 on page 2 of the above-identified Office Action, claims 1-38 have been rejected as being anticipated by Kau et al. (U.S. Patent No. 6,421,754) (hereinafter "Kau") under 35 U.S.C. § 102(e).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 11, line 23 to page 12, line 4 of the specification and in the original claims of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a program-controlled unit, having:

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting the intelligent core and the units, including an interface connection between the intelligent core and the internal peripheral units, between the intelligent core and the external peripheral units, between the intelligent core and the memory devices, and between the plurality of units; and

the **structurable hardware unit having direct connections and configurable data paths and data linkage paths between devices to be connected by the structurable hardware unit.** (emphasis added)

According to the present invention, the structurable hardware unit 12 (SLE layer) is arranged between the intelligent core or µP core 11, peripheral units (for example the peripheral units 13 to 19) provided inside and/or outside the program-controlled unit, and/or memory devices (for example the RAM 2 and/or the ROM 3) (see Fig. 1). The unit contains **structurable** data paths and/or logic elements which can be structured or configured in such a way that the structurable hardware unit 12 can be used as a **configurable** intelligent interface between the µP core and one or more peripheral units and/or between the intelligent core and one or more memory devices and/or between two or more peripheral units themselves and/or between one or more peripheral units and one or more memory devices.

The structurable hardware unit 12, shown in Fig. 2, has a clock generation unit and a logic block unit 122, which is the actual core of the unit 12. Logic block unit 122 is extremely flexible. Virtually **any** desired linkages, processing and evaluations of the input signals can be carried out by such universally usable structurable logic arrangements (page 16, line 19 through page 17, line 2). Logic block 122 is divided into sub-blocks. The sub-blocks are configurable multiplexers (**for switching data paths** as desired), registers (for buffer-

storing data and/or coded states) and structurable logic (for linking data and/or signals with one another and with constants and for coding and decoding states).

Because within the SLE layer 12, there are both direct connections and configurable data paths and data path linkages between the devices which are connected or can be connected via the SLE layer, if the structurable hardware unit 12 has access to memory devices (for example to the RAM 2 and/or to the ROM 3) it can transfer data from and to the memory devices **independently**, i.e. **without the participation of the intelligent core**, for itself and/or the core and/or the peripheral units. As a result, data transfers can be carried out more rapidly and without burdening the µP core 11. In this case, the structurable hardware unit 12 is constructed in such a way that it can identify and handle contending accesses to memory devices.

The Kau reference discloses a computer docking station (Fig. 1), that allows a computer to easily be connected to a variety of peripheral devices (Fig. 3 and col. 9, lines 2-63). As explained in col. 10, lines 41-52, the docking station provides A) advantageous system expandability through i) ISA/EISA slots, ii) additional HDD space, CDROM, multimedia

with monaural, stereo, quadraphonic and other sound systems, and iii) wide bandwidth PCI bus 71 local bus slots. A further area of advantage B) is quick, easy connections to desired non-portable equipment through i) easier to use, bigger keyboard, ii) bigger, higher quality, CRT display iii) better mouse, printer, and so on. For example, the user merely pushes the notebook 6 into the docking station 7 quickly and easily, and all peripherals are then hooked up, without any further user hookup activity.

As shown in Fig. 3 of Kau, bus 104 connects microprocessor unit (MPU) 102 with the above-mentioned peripheral devices. A block diagram of MPU 102 is shown in Fig. 9. A DOS-compatible static 486 core in MPU 102 allows on-the-fly clock-scale and clock-stop operation to conserve battery power (col. 12, lines 58-66). The MPU 102 is suitably a static device wherein no internal data is lost when the clock input is stopped or clock-modulated by turning the clock off and on repeatedly (col. 13, line 66 through col. 14, line 2).

As is explained in col. 13, lines 59-66, power management block 708 provides a dramatic reduction in current consumption when the microprocessor MPU 102 is in standby mode. Low voltage operation, such as 3.3 volts or less, coupled with power management, provides the capability to achieve low

system battery power consumption (col. 12, lines 58-66). Standby mode is entered either by a hardware action in unit 920 of PPU 110 or by a software initiated action. Standby mode allows for CPU clock modulation, thus reducing power consumption. MPU power consumption can be further reduced by generating suspend mode and stopping the external clock input.

More specifically, as recited in col. 14, lines 7-22 of Kau, core 702 simply has a system-management mode with an additional interrupt and a **separate address space** that is suitably used for **system power management or software transparent emulation of I/O (input/output) peripherals**. The system management mode is entered using a system management interrupt, which has a higher priority than any other interrupt and is maskable. While running in the **separate address space**, the system management interrupt routine advantageously executes without interfering with the operating system or application programs. After reception of the system management interrupt, portions of the CPU are automatically saved, system management mode is entered and **program execution begins in the separate address space**. (col. 14, lines 7-22).

Kau simply provides a software controlled power management circuit configuration that adjusts the speed of the core of a microprocessor unit. Kau does not have an SLE layer or

structurable hardware unit 12 according to the present invention. In Kau, the peripheral devices are connected directly to MPU 102 via main bus 71, interconnected to bus 104 (col. 8, line 66 through col. 9, line 2). In contrast, the SLE layer 12 of the present claimed invention has structurable data paths and/or logic elements which can be structured or configured in such a way that the SLE layer 12 can be used as a configurable intelligent interface between the intelligent core and one or more peripheral units and/or between the µP core and one or more memory devices and/or between two or more peripheral units themselves and/or between one or more peripheral units and one or more memory devices. Moreover, the SLE layer can transfer data from and to the memory devices independently of the intelligent core which is not disclosed in Kau. Nor does Kau disclose a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal as recited in the instant claims.

Clearly, Kau does not show "said structurable hardware unit having direct connections and configurable data paths and data linkage paths between devices to be connected by said structurable hardware unit" as recited in independent claim 1 of the instant application.

Nor does Kau show "said structurable hardware unit including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal" as recited in independent claim 20.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 20.

Moreover, the references do not show that "said structurable hardware unit is configured for access to said memory devices independently of said intelligent core and for evaluating and processing data and signals received thereby, said structurable hardware unit including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal" as recited in new dependent claim 77, or that "said structurable hardware unit has direct connections and configurable data paths and data linkage paths between devices to be connected by said structurable hardware unit, and said structurable hardware unit is configured for access to said memory devices independently of said intelligent core and for injecting instructions into said

instruction pipeline of said intelligent core" as recited in new dependent claim 78.

In view of the foregoing, reconsideration and allowance of claims 1-38 and new dependent claims 77-78 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Enclosed is a credit card payment form including $36.00 to cover the additional dependent claims in excess of the amount already paid for in the subject application.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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